

PHASE INTERPOLATOR AND RECEIVER

CROSS REFERENCE TO RELATED APPLICATIONS

This application claims benefit of priority under 35
5 USC 119 based on Japanese Patent Application No. P2003-086293
filed on March 26, 2003, the entire contents of which are
incorporated by reference herein.

BACKGROUND OF THE INVENTION

10 1. Field of the Invention

The present invention relates generally to a phase interpolator and receiver, and more particularly, to a phase interpolator and receiver capable of ensuring operations to adjust clock phases into data phases.

15 2. Description of Related Art

Figure 11 is a block diagram showing a high-speed input/output (I/O) device. A transmitter 4 converts input parallel data 1 into serial data 2. In this specification, the serial data is differential pair signals from CML (current mode logic). The converted serial data 2 is transmitted to a receiver 5. The receiver 5 receives the serial data 2 and converts it into parallel data 3. The serialization of parallel data into serial data and the deserialization of serial data into parallel data are carried out in synchronization with clock signals. The serial data 2 from the transmitter 4 is asynchronous with the clock signals of

the receiver 4. To correctly read the serial data 2 in the receiver 5, the serial data 2 must be synchronized with the clock signals. To achieve this, the phases of the clock signals must be adjusted to those of the serial data 2. To 5 provide a function of adjusting the phases of clock signals to those of serial data, a phase interpolator (abbreviated as PI) and a data read circuit are employed.

Figure 12 is a timing chart showing serial data 2' supplied to a data read circuit and four-phase clock signals 10 provided from a phase interpolator to the data read circuit. Among the four-phase clock signals, the signals Reclock_InIP 91 (positive = 0) and Reclock_InIN 93 (negative = 0) hit waveform centers of the serial data 2', to correctly read the serial data 2'. If these clock signals hit the serial data 15 2' shift, the serial data 2' will incorrectly be read causing malfunctions in a receiver.

The signals Reclock_InIP 91 and Reclock_InIN93 form a pair. Shifted from these signals by 90 degrees are signals Reclock_InQP and Reclock_InQN that form another pair.

20 Figure 13 is a timing chart showing the clock signals Reclock_InIP 91 and Reclock_InIN 93 that have an improper duty ratio deviating from a proper duty ratio of 50:50 due to, for example, noise. The clock signal Reclock_InIP 91 hits a waveform center of the serial data 2'. The clock signal 25 Reclock_InIN 93, however, hits a data transient position of the serial data 2' due to the duty ratio deviation. This will

cause a data read error.

Figure 14 is a schematic view showing an output circuit of a phase interpolator according to a related art. A mixer 52 provides signals 61. These signals are slewed by an 5 integrator 62, and the slewed signals are sent to an output buffer 63. The output buffer 63 amplifies the signals and provides output signals 65. The output signals 65 are sent to a data read circuit (not shown) and to a duty cycle correction circuit (DCC) 64 to correct duty ratios. The DCC 10 64 feeds duty correction signals back to the signals 61. The DCC 64 is capable of correcting the duty ratios of the signals 61.

The phase interpolator according to the related art, however, causes fluctuations in the voltage of the signals 15 61 due to parasitic capacitance and coupling capacitance that are affected by the operation of peripheral circuits.

Figure 15 is a diagram showing signals 61' that are affected by voltage fluctuations. The signals 61' involve varying positive and negative voltage levels that move 20 oppositely due to the CML (current mode logic), causing a small swing zone of reduced amplitude. The small swing zone is insufficiently amplified by the output buffer 63, and therefore, will not be recognized as a clock pulse by a data read circuit. In addition, the voltage variations 25 deteriorate duty ratios, making the data read circuit unable to correctly read data.

SUMMARY OF THE INVENTION

An aspect of the present invention provides a phase interpolator for adjusting a phase of differential clock signals of a receiver to a phase of data from a transmitter

5 that includes, an integrator configured to slew edges of differential clock signals adjusted to the phase of the data from the transmitter, a output buffer configured to amplify an output of the integrator, a duty cycle correction circuit configured to feed duty correction signals back to the adjusted

10 differential clock signals, and a controller configured to ensure operations of an amplitude of the output buffer and a data read circuit to adjust the swings and duties of the adjusted differential clock signals.

Another aspect of the present invention provides a phase interpolator that includes, an integrator configured to receive adjusted differential clock signals, the integrator configured to slew the differential clock signals, a output buffer configured to amplify an output of the integrator, a duty cycle correction circuit configured to receive amplified signals from the output buffer to adjust phases of the amplified signals, the duty cycle correction circuit configured to feed the adjusted signals back to the output buffer, and a controller configured to control a rate of slewing the differential clock signals carried out by the

20 integrator, when swings of the differential clock signals are below a predetermined value.

Another aspect of the present invention provides a receiver that includes, a digital-analog converter configured to convert an inputted signal into a current, a mixer configured to receive an output of the digital-analog converter and a 5 clock, the mixer configured to shift a phase of the clock according to the output of the digital-analog converter to output adjusted differential clock signals, an integrator configured to receive data and adjusted differential clock signals, the integrator configured to slew the differential 10 clock signals, a output buffer configured to amplify an output of the integrator, a duty cycle correction circuit configured to receive amplified signals from the output buffer to adjust a phase of the amplified signal, the duty cycle correction circuit configured to feed the adjusted signals back to the 15 output buffer, and a controller configured to control a rate of the slewing the differential clock signals carried out by the integrator, when swings of the differential clock signals are below a predetermined value, and a data read unit configured to read data using the output of the output buffer.

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BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a block diagram showing a receiver according to an embodiment of the present invention;

Figure 2 is a schematic view showing the phase 25 interpolator 7 according to the embodiment;

Figure 3 shows the output circuit 53 according to the

embodiment;

Figure 4 is a circuit diagram showing examples of the controller 71 and integrator 62 according to a first embodiment of the present invention;

5 Figure 5 shows an example of the operational amplifier 21 of Fig. 4;

Figure 6 shows an example of one of the operational amplifiers 40a and 40b of Fig. 5;

10 Figure 7 explains amplitude expansion according to the embodiment;

Figure 8 is a circuit diagram showing examples (71a, 62a) of the controller 71 and integrator 62 according to a second embodiment of the present invention;

15 Figure 9 is a circuit diagram showing examples (71b, 62b) of the controller 71 and integrator 62 according to a third embodiment of the present invention;

Figure 10 shows another example (62c) of the integrator 62. This example halves the capacitance of the integrator 62c in an OFF operation, instead of completely disconnecting the 20 capacitance;

Figure 11 is a block diagram showing a high-speed input/output (I/O) device;

Figure 12 is a timing chart showing serial data 2' supplied to a data read circuit and four-phase clock signals 25 provided from a phase interpolator to the data read circuit;

Figure 13 is a timing chart showing the clock signals

Reclock_InIP 91 and Reclock_InIN 93 that have an improper duty ratio deviating from a proper duty ratio of 50:50;

Figure 14 is a schematic view showing an output circuit of a phase interpolator according to a related art; and

5 Figure 15 is a diagram showing signals 61' that are affected by voltage fluctuations.

DETAILED DESCRIPTION OF EMBODIMENTS

Various embodiments of the present invention will be
10 described with reference to the accompanying drawings. It is to be noted that the same or similar reference numerals are applied to the same or similar parts and elements throughout the drawings, and the description of the same or similar parts and elements will be omitted or simplified.

15 Figure 1 is a block diagram showing a receiver according to an embodiment of the present invention. The receiver includes a data read circuit 6 and a phase interpolator 7. The phase interpolator 7 receives four-phase ($0, \pi/2, \pi, 3\pi/2$) clock signals (Clock_In, CML) 8 and provides four-phase clock
20 signals (Reclock_In) 9 whose phases are synchronous with those of serial data 2'. The serial data 2' is sent from a transmitter (not shown) to the data read circuit 6. The data read circuit 6 reads the serial data 2' based on the clock signals 9, provides the phase interpolator 7 with a phase
25 information signal (UP/DN) 10 containing information about the phases of the clock signals and serial data 2', and outputs

data 11, which is synchronous with clock signals in the receiver, and clock signals 9', which have phases adjusted to those of the data 11, to subsequent circuits for further processing.

5 Figure 2 is a schematic view showing the phase interpolator 7 according to the embodiment. The phase interpolator 7 has an IDAC (switched current digital to analog converter) controller 51 to convert an input signal into a current output 56, a mixer 52 to receive the output 56 of the
10 IDAC controller 51 and the clock signals 8, shift the phases of the clock signals 8 according to the output 56, and provide differential clock signals, and an output circuit 53 to receive the outputs of the mixer 52.

The phase information signal 10 from the data read
15 circuit 6 (not shown in Fig. 2) is received by the IDAC controller 51, which converts the signal 10 into the current signal 56 indicative of an up/down current value. The four-phase clock signals 8 are received by the mixer 52, which mixes the clock signals 8 with the current signal 56, shifts
20 the phases of the clock signals 8, and provides the phase-shifted clock signals to the output circuit 53.

Figure 3 shows the output circuit 53 according to the embodiment. The output circuit 53 has an integrator 62 to receive and modify the differential clock signals 61 whose
25 phases have been adjusted to those of data, an output buffer 63 to amplify the outputs of the integrator 62, a duty

correction circuit 64 to receive the amplified signals from the output buffer 63, adjust the phases of the received signals, and feed phase adjusted signals back to the output buffer 63, and a controller 71 to control the modification carried out 5 by the integrator 62 on the differential clock signals 61. The controller 71 checks to see if the voltage of the output signals 61 from the mixer 52 is amplifiable by the output buffer 63, and according to a result of the checking, changes the capacitance of the integrator 62. The integrator 62 makes a 10 signal incline so as to reduce the influence of phase shift by phase insertion. Namely, the integrator 62 makes a signal waveform more slewed. By changing the capacitance of the integrator 62, it is possible to control the rising speed of each clock signal edge and restore the amplitude of each clock 15 signal to a voltage level that is amplifiable by the output buffer 63. The output circuit 53 handles one differential clock pair among the four-phase clock signals 61. The phase interpolator 7 incorporates two systems, one for a differential clock pair of 0 and 180 degrees and the other 20 for a differential clock pair of 90 and 270 degrees. Namely, in the phase interpolator 7, a combination of the output circuit 53, mixer 52, and IDAC controller 51 is prepared for the differential clock pair of 0 and 180 degrees, and another combination of the same is prepared for the differential clock 25 pair of 90 and 270 degrees. The following explanation is conducted only for one of them, and it should be understood

that the same explanation is applicable to the other.

Figure 4 is a circuit diagram showing examples of the controller 71 and integrator 62 according to a first embodiment of the present invention. The controller 71 has an operational amplifier 21, a capacitor 12, and an inverter 13. The integrator 62 has an NMOS transistor 14a connected to one (61a) of the differential clock signals, a capacitor 15a connected to the NMOS transistor 14a, an NMOS transistor 14b connected to the other (61b) of the differential clock signals, and a capacitor 15b connected to the NMOS transistor 14b. The operational amplifier 21 finds a difference between the positive signal 61a or Integp and the negative signal 61b (an inverted signal due to the CML) or Integn. The operational amplifier 21 then compares the found differential voltage with a reference signal 17 or Vref. If the differential voltage is smaller than the reference signal Vref, the operational amplifier 21 provides a detected signal. Here, the capacitor 12 is able to prevent a switching of the inverter 13 upon first receiving a detected signal. Namely, only when the differential voltage is smaller than the reference signal Vref several times, does the output of the operational amplifier 21 make the voltage of a node 18 exceed a threshold of the inverter 13, so that the inverter 13 may provide an OFF signal to a line 19. The OFF signal turns off the NMOS transistors 14a and 14b so as to disconnect the capacitors 15a and 15b of the integrator 62. As a result, the capacitance of the

integrator 62 decreases, quickening the rise of each clock edge and restoring the amplitude of the clock signals. Here, capacitance means a function of accumulating charge and includes wiring load capacitance and input terminal
5 capacitance.

According to the embodiment, the capacitor 12 accumulates a predetermined amount of charge. According to another embodiment, the capacitor 12 may be omitted. In this case, a single pulse of a detected signal makes the voltage
10 of the node 18 exceed the threshold of the inverter 13, thus providing an OFF signal to the line 19. In this way, if it is necessary to invert a signal after one or a small number occurrences of the differential voltage becoming smaller than the reference signal Vref, the capacitor 12 can be omitted
15 or replaced with a smaller one. If it is necessary to invert a signal after a larger number of times of such occurrence, the capacitor 12 can be replaced with a larger one.

Figure 5 shows an example of the operational amplifier
21 of Fig. 4. According to this example, the operational
20 amplifier 21 has operational amplifiers 40a and 40b. Each of the operational amplifiers 40a and 40b finds a difference between a positive signal 41 and a negative signal 42 and compares the difference with a reference signal 43. If any
25 one of the differences "positive signal 41 - negative signal 42" and "negative signal 42 - positive signal 41" is smaller than the reference signal 43, an exclusive OR gate 45 causes

an inversion to provide a high output signal 46. This results in accumulating charge in the capacitor 12. If this consecutively occurs several times, the accumulated charge exceeds the threshold of the inverter 13, which then provides
5 an inverted signal.

Figure 6 shows an example of one of the operational amplifiers 40a and 40b of Fig. 5. An operational amplifier 81 compares the positive signal 41 with the negative signal 42 and provides a difference between them as a signal 83. An
10 operational amplifier 82 compares the signal 83 with the reference signal 43. If the signal 83 is greater than the reference signal 43, it is considered that the signals are amplifiable by the output buffer 63, and the amplifier 82 provides a high output signal 84, which is inverted by an
15 inverter 85 into a low signal 44. If the operational amplifier 82 determines that the signal 83 is lower than the reference signal 43, it is determined that the signals are not amplifiable by the output buffer 63. Then the operational amplifier 82 provides a low output signal 84, which is inverted
20 by the inverter 85 into a high output signal 44.

Figure 7 explains amplitude expansion according to the embodiment. In the controller 71, the voltage of the node 18 may exceed the threshold of the inverter 13, to provide an OFF signal to the line 19. This OFF signal turns off the NMOS
25 transistors 14 to disconnect the capacitors 15 of the integrator 62. This reduces the capacitance of the integrator

62, quickening the rise of each clock edge and restoring the amplitude of each clock signal. This controls changes exerted by the integrator 62 on the differential clock signals, expands amplitude (dot-and-dash lines) more than the related art
5 (solid and broken lines), and enables all signals to be amplified by the output buffer 63. Consequently, the embodiment allows the data read circuit 6 to correctly recognize all clock signals and correctly read data, prevents the destruction of duty ratios of clock signals due to phase
10 shift in the clock signals, and ensures data read operation through phase adjustment between data and clock signals.

Figure 8 is a circuit diagram showing examples (71a, 62a) of the controller 71 and integrator 62 according to a second embodiment of the present invention. Compared with Fig. 4,
15 the controller 71a has two operational amplifiers 21a and 21b that receive different reference signals Vref1 and Vref2, respectively. The operational amplifier 21a finds a difference between the signals Integp and Integn and compares the differential voltage with the reference signal Vref1. If
20 the differential voltage is smaller than the reference signal Vref1, a predetermined amount of charge is accumulated in a capacitor 12a. On the other hand, the operational amplifier 21b finds a difference between the signals Integp and Integn and compares the differential voltage with the reference signal Vref2. If the differential voltage is smaller than the
25 reference signal Vref2, a predetermined amount of charge is

accumulated in a capacitor 12b. Based on these different standards, the operational amplifiers 21a and 21b turn off NMOS transistors 14 and disconnect capacitors 15 of the integrator 62a. For example, the reference signals Vref1 and

5 Vref2 are set to $V_{ref1} > V_{ref2}$. The operational amplifier 21b that receives the reference signal Vref2 may have no capacitor. That results that an inverter 13b inverts in response to a single input pulse. The capacitors 15a and 15b and the capacitors 15c and 15d may have different capacitance values.

10 That results in differ load of the capacitance when the NMOS transistors 14 are turned off. According to the capacitance of the disconnected capacitors, the rising speed of each clock edge changes so as to control the degree of restoration of clock amplitude. This technique realizes precise control of

15 clock amplitude.

Figure 9 is a circuit diagram showing examples (71b, 62b) of the controller 71 and integrator 62 according to a third embodiment of the present invention. The controller 71b has an operational amplifier 22a that receives the signals Integp,

20 Integn, and Vref1, an operational amplifier 22b for receiving the signals Integp, Integn, and Vref2, a delay circuit 25 for delaying the output of the operational amplifier 22b, a flip-flop (FF) for receiving the output of the delay circuit 25 at a clock input terminal and the output of the operational amplifier 22a at an input terminal, an inverter 26 for inverting the output of the delay circuit 25, a flip-flop 24

for receiving the output of the inverter 26 at a clock input terminal and the output of the flop-flop 23 at an input terminal, and a NAND gate 27 for receiving the outputs of the flip-flops 23 and 24 and providing a NAND of the received signals. The 5 controller 71b is an example of a counter circuit. The operational amplifier 22a receives the signals Integp and Integn (61a and 61b), finds a difference between them, and compares the difference with the reference signal Vref1. If the difference is smaller than the reference signal Vref1, 10 the operational amplifier 22a provides an output signal 33. Similarly, the operational amplifier 22b finds a difference between the signals Integp and Integn and compares the difference with the reference signal Vref2. Here, the reference signal Vref2 is set to have a voltage level that 15 always generates clock signals. Accordingly, an output signal 34 from the operational amplifier 22b generates clock signals. The operational amplifiers 22a and 22b may have the same structures as those of Figs. 5 and 6. The output signal 34 is slightly delayed by the delay circuit 25 so that the 20 output signal 33 is properly received by the FF 23. The signal 33 hit by a clock signal 35 from the delay circuit 25 is sent to the next FF 24. The clock signal 35 is inverted by the inverter 26, and a half-clock-shifted clock signal 36 hits the FF 24, which provides a signal 38. Signals 37 and 38 are 25 passed to the NAND gate 27. During a high period of the signal 33, i.e., only when voltage variations are outside of an

allowable range, does the NAND gate 27 provide a low signal
39 to turn off NMOS transistors 28a and 28b and disconnect
capacitors 29a and 29b of the integrator 62b. This reduces
the capacitance of the integrator 62b, quickening the rise
5 of each clock edge and restoring clock amplitude. This
embodiment employs two flip-flop stages so that a switching
operation may take place only when the reference signal 31
has been exceeded at least two times. It is possible to employ
three, four, or more flip-flop stages, so as to trigger a
10 switching operation upon three or more occurrences of
exceeding the reference signal. In this way, the
configuration of Fig. 9 is capable of defining the number of
occurrences necessary to trigger a switching operation. The
structure of Fig. 9 can turn off the NMOS transistors 28a and
15 28b upon two occurrences of the difference between the signals
Integp and Integn (61a and 61b) being below the reference
signal Vref1. It is thus possible to optionally set the number
of occurrences of the difference between the signals Integp
and Integn being lower than the reference signal Vref1 to turn
20 off the NMOS transistors 28a and 28b.

Figure 10 shows another example (62c) of the integrator
62. This example halves the capacitance of the integrator 62c
in an OFF operation, instead of completely disconnecting the
capacitance. More precisely, one capacitor 15e of the
25 integrator 62c is configured so as to be switched off with
an NMOS transistor 14e, and the other capacitor 14f thereof

is fixed. Even if the NMOS transistor 14e is turned off so as to disconnect the capacitor 15e, the capacitor 15f remains active, thus restricting the rise of each clock edge.

Although this example employs only one switching element, 5 more reference signals and more switching stages may be employed in order to precisely control the capacitance of the integrator. Voltage applied to the switching elements may analogously be controlled in response to a voltage difference between the signals 61, in order to analogously control the 10 capacitance of the integrator.

As explained above, the phase interpolator and receiver according to any one of the embodiments of the present invention determine, with a controller incorporated in the phase interpolator, whether or not the voltage of signals from 15 a mixer is amplifiable by an output buffer, and according to a result of the determination, change the capacitance of an integrator incorporated in the phase interpolator. By changing the capacitance of the integrator, the phase interpolator controls the rising speed of each clock edge and 20 restores the amplitude of clock signals so that the clock signals may have voltage levels amplifiable by the output buffer. This results in providing correct clock signals that correctly hit data in a data read circuit and ensure the normal operation of the receiver.

25 The present invention may be embodied in other specific forms without departing from the spirit or essential

characteristics thereof. The embodiments are therefore to be considered in all respects as illustrative and not restrictive, the scope of the present invention being indicated by the appended claims rather than by the foregoing description, and
5 all changes which come within the meaning and range of equivalency of the claims are therefore intended to be embraced therein.